REMARKS

Claims 17-20 are pending in this application. Claims 17-20 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Lepejian et al. This rejection is respectfully traversed.

Claims 17-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Lepejian et al. in the March 26, 2003 Office Action. In response to Applicants' reply, the July 10, 2003 Office Action indicated, "claims 17-20 are in condition for allowance" (see page 2, the paragraph titled "Response to Amendment"). However, in the present Office Action, claims 17-20 have been rejected again based on the same reference, Lepejian et al., and exactly the same reasons asserted by the Examiner in the March 26, 2003 Office Action. The Examiner did not provide any specific reason why the allowance of claims 17-20 should be withdrawn in the present Office Action.

In response, Applicants first emphasize that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention under 35 U.S.C. §103 for lack of the requisite factual basis. Copying the assertion in the March 26, 2003 Office Action does not provide any reason why claims 17-20 are obvious over Lepejian et al. and the allowance of claims 17-20 should be withdrawn. This is so because the Examiner admitted that the rejection of claims 17-20 based on the reason asserted in the March 26, 2003 Office Action, could not be maintained (see the July 10, 2003 Office Action). The Examiner has not discharged his burden to establish a *prima facie* case of obviousness.

Second, Lepejian et al. does not teach a method of executing testing of a memory cell array and a method of providing data read out from a memory cell array including all the limitations recited in claims 17-20. The following is reproduction of Applicants' arguments

made on page 13 of the June 25, 2003 reply, in response to which the Examiner allowed claims 17-20 in the July 10, 2003 Office Action.

> *Independent claim 17 is directed to a method of loading to an instruction memory that stores the instruction to the ALPG generating a memory test pattern. Loading is terminated when there is a data end instruction in the loading data. The feature is provided to quickly end the loading when the data to be loaded (memory test pattern generated by ALPG) is short to reduce the overhead time required for test preparation. In a BIST with a programmable ALPG as in the present invention, the method of reducing the time required to load into an instruction memory is an important distinction. Lepejian does not disclose such an instruction memory. Withdrawal of the rejection of claim 17 and its dependent claim 18, therefore, is respectfully solicited.*
>
> *Independent claim 19 requires read out from a memory cell array in synchronization with a first clock signal of a first frequency to an external circuit that operates in synchronization with a second clock signal of a lower frequency. Dependent claim 20 is directed to scrambling the address so as to exchange the order of data output from the device, facilitating determination at the ATE side of low speed in the case where the output of a memory device operating at high speed in independent claim 19 is determined using the low speed ATE. If this feature is not present at the device (BIST) side, determination at the ATE side is rendered difficult. This means that AT speed testing which is a test that operates the memory device at a higher speed than the ATE cannot be realized. Although the ATE for a memory generally has an address scramble function, the scramble cannot be altered by the writing or reading operation with respect to the device. This feature is employed since information of errors corresponding to the address in the memory device must be taken in the ATE in order to conduct remedy analysis of the memory device having redundancy. As Lepejian lacks teaching or suggestion of these features, withdrawal of the rejection of claims 19 and 20 is respectfully solicited.*

Thus, consideration of the teachings of Lepejian et al. does not teach or suggest each and every limitation of claims 17-20. In the instant case, the pending rejection has not established *prima facie* obviousness of the claimed invention as recited in claims 17-20, because the Examiner failed to provide any specific reason why allowed claims 17-20 should be rejected, and Lepejian et al. fails to teach all the claim limitations within the meaning of 35 U.S.C. §103. Applicants, therefore, solicit withdrawal of the rejection of claims 17-20 and favorable consideration thereof.

On May 25, 2005, Applicants contacted Examiner Chaudry to discuss the reason why he had rejected claims 17-20 again. Examiner Chaudry suggested that Applicants should file the response to the present Office Action first, and then, contact the Examiner to have an interview. Accordingly, the Examiner will be contacted by Applicants for an interview.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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